Serial Number: 09/808750 Filing Date: March 15, 2001

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Title: DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR MEMORY DEVICES

## REMARKS

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Applicant has carefully reviewed and considered the Office Action mailed on March 7, 2003, and the references cited therewith.

No claims are amended or cancelled. Claims 1-54 remain pending in this application.

## \$103 Rejection of the Claims

Claims 1-54 were rejected under 35 USC § 103(a) as being unpatentable over Tanoi (U.S. Patent No. 5,708,621).

The pending office action states on page 5 that:

Tanoi does not explicitly depict a width of the strapping line being greater than a width of the wordlines as now included in the independent claims 1, 5, 8, 15, 19, 26, 30, 37, 42, 45, and 49. As is well-known in the art, a wider conductor has lower resistance. Tanoi shows in one embodiment in figures 16-18, a strapping line 118 having low resistance (column 9, lines 33-41) and gaps between the strapping lines are large to accommodate wider strapping lines.

Applicant agrees with the Examiner that Tanoi does not disclose a width of a strapping line that is greater than a width of the wordlines. However, Applicant respectfully traverses that such differences in width are obvious. Within the numerous constraints of an ultra large scale integrated (ULSI) circuit, increasing a width of a line is not always possible given other negative effects. For example, Applicant's specification on page 1, lines 21-26 notes that, "even though a low resistance metal may be chosen for a conductor, the size of the cross section of a conductor affects its resistivity, and neighboring structures may create a capacitance that causes additional resistance in the conductor." Applicant respectfully submits that the designs taught in the present specification overcome these technical hurdles and permit a width of a strapping line that is greater than a width of the wordlines.

Applicant respectfully submits, any assertion that a width of a strapping line that is greater than a width of the wordlines is obvious, given the constraints of an ultra large scale integrated (ULSI) circuit, is using impermissible hindsight. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir.

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1991); MPEP § 2143. The Examiner must avoid hindsight. In re Bond, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990).

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In contrast, Applicant's independent claims 1, 5, 8, 15, 19, 26, 30, 37, 42, 45, and 49 all include a width of a strapping line that is greater than a width of the wordlines. Because, as stated by the Examiner, the single Tanoi reference, does not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 1, 5, 8, 15, 19, 26, 30, 37, 42, 45, and 49. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

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## **CONCLUSION**

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this day of June, 2003.

Gina M. Uphus	Kha Ophus
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Name	Signature